RSRE
MEMORANDUM No. 4561

ROYAL SIGNALS & RADAR ESTABLISHMENT

A DIGITAL SATELLITE DELAY SIMULATOR

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Title: A digital satellite delay simulator

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Date: December 1991

SUMMARY

This document describes the design and operation of a bi-directional digital satellite delay simulator. The data rates which are catered for are 2400, 3600, 7200 and 16000 bps, but other data rates could be included with only minor modification.

The circuit is based on the Motorola 6809 microprocessor which uses the Motorola 6852 synchronous serial data adapter (SSDA) as the interface devices.

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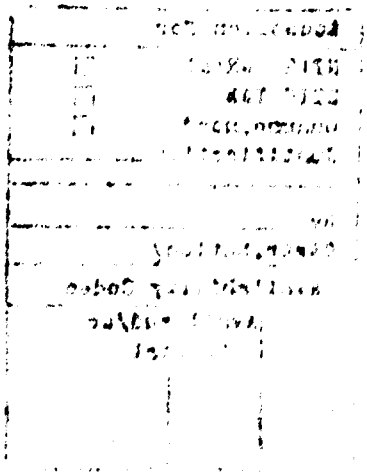

1. Introduction

When using a satellite as part of a communications system, there is a delay introduced due to the signal propagation time to the satellite and back. This time delay is approximately one quarter of a second and is calculated thus:-

propagation time = distance travelled/velocity of light
=7.2x10^7 mtrs / 3x10^8 mtrs sec^-1
= approx. 1/4 seconds (per link)

This time delay can cause problems in certain situations such as when packets are used as a transmission protocol.

The way a packet system works is to send out numbered data packets and then to wait until the receiver acknowledges the correct reception of each packet, unacknowledged packets need to be retransmitted. For each data protocol there is a specified maximum number of unacknowledged packets which can be in transit at any one time, therefore if the satellite delay slows down the receivers' acknowledgements, the packet throughput will be reduced.

There may seem little point in using packet protocols for satellite communications but the main advantage is that any packet which has been acknowledged is guaranteed error free.

This satellite delay project is intended to assist research into different packet protocols by simulating the satellite delay, which means that a 'live' broadcast is not required and thus releases air time, and equipment, for operational traffic. Fig 1 shows the delay box in operation.

The report is split into two sections, these being hardware and software, they are described in the following report.

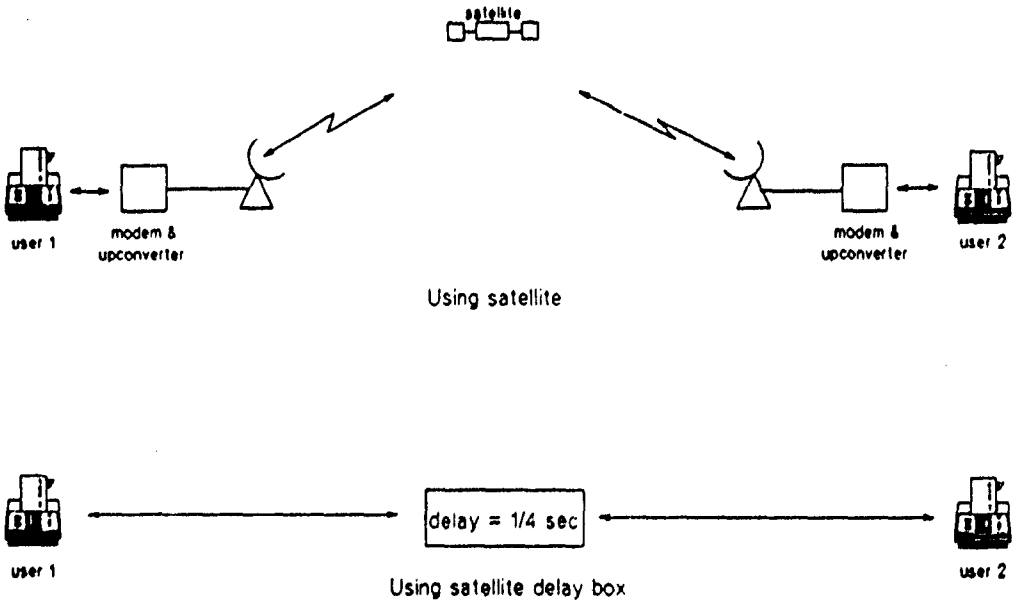

Fig 1 operation of delay box

2. Hardware

The hardware is based on the Motorolla 6809 microprocessor which utilises two Motorolla 6852 Synchronous Serial Interface Adapters (SSDA), for bi-directional operation, as the data interfaces. Fig 2 shows the functional circuit diagram of the delay box.

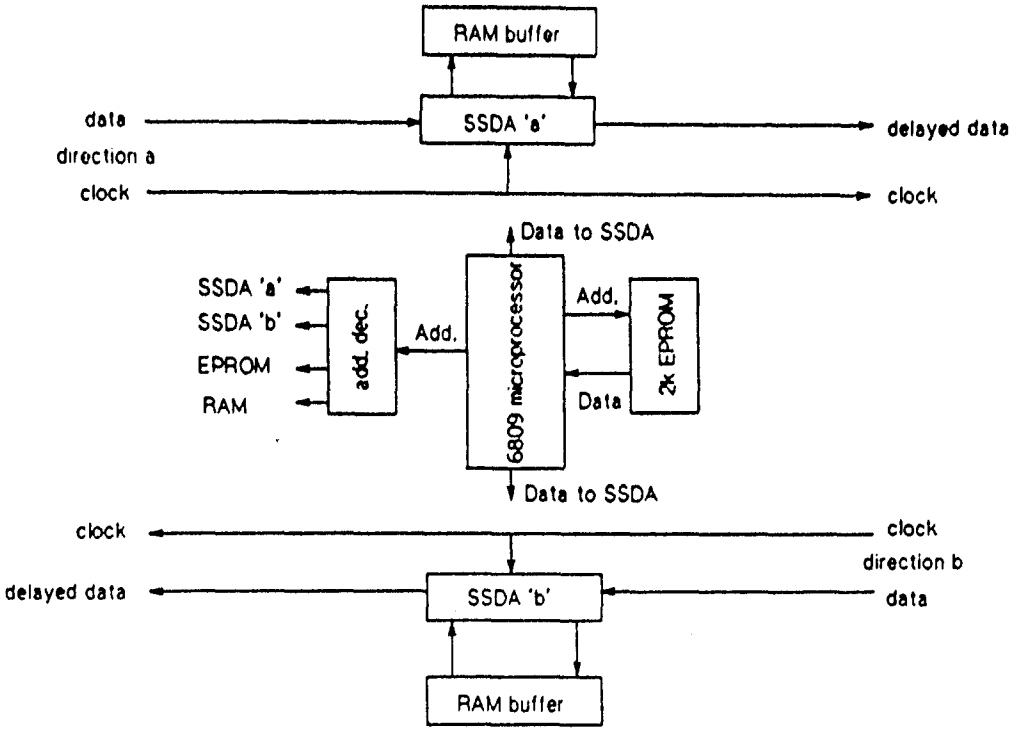

Fig 2 functional cct diagram

2.1 Operation

The operation of this full duplex delay box is described here in one direction but the operation is identical in both directions. The serial data and clock are presented to the SSDA (via a line receiver) and, after being configured (see software section for configuration details), the SSDA will start to put the data into its' internal receive buffer. When the 8 bit buffer is full the receive register is parallel loaded into the first of the SSDA's holding registers and, depending whether the SSDA is set up for a one byte or two byte transfer, will set the appropriate flag in the SSDA's status register. If the SSDA is set up for a two byte transfer then two bytes will need to be transferred from the receive register before the flag is set in the SSDA status register.

The microprocessor is continually polling the status registers

of the two SSDA's (because it has nothing else to do!) and, when a receiver register full flag is found set in either SSDA, the appropriate service routine is carried out.
The serial data has to be delayed by one quarter of a second before it is retransmitted, the storage elements used for this are two 2114 1k x 4 bit RAM i/c's (see software section for more detail). The RAM is cycled round continually in an endless loop and it is the length of this loop, for a given data rate, which determines the length of the delay. The actual loop length is determined by the value of a constant set, in the program, by the programmer.

To allow more than one data rate to be catered for, there are four programs, each with appropriate constant values, stored in EPROM, which can be selected by a thumbwheel switch. This works by using the thumbwheel switch to select one of the four 512 byte pages which are in the EPROM. Fig 3 shows this.
The 64k possible addressing space is partially decoded into four 16k areas. The address decoding is done using a 74153 two to four line decoder. The memory map is shown overleaf in fig 4.

The circuit is packaged in a diecast box with an integral mains operated power supply. The serial data streams are connected to the delay box via two 25 way 'd' type connectors, there is also means to remove the delay in either or both directions by a toggle switch.

3. Software

The software for the project was written on the Hewlett Packard

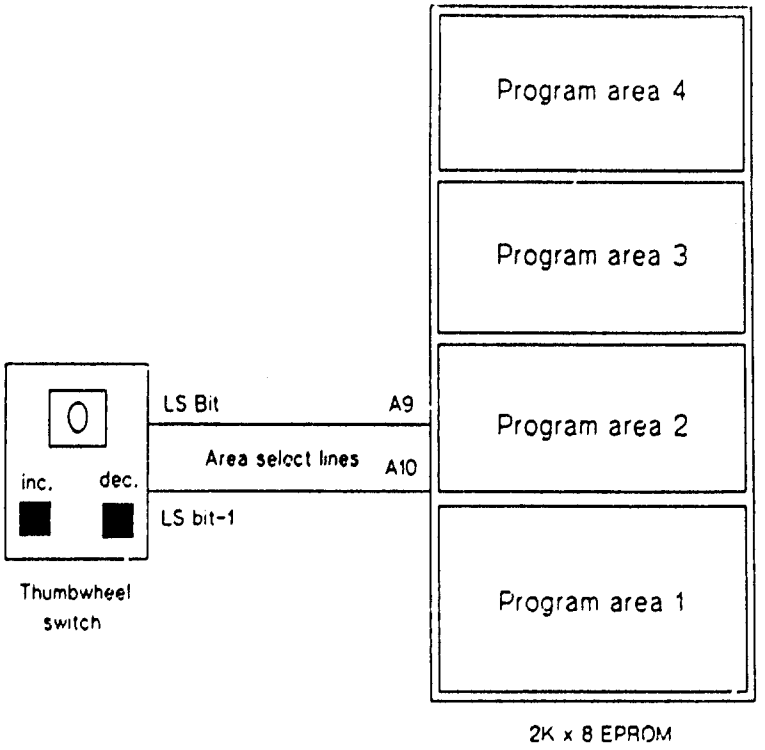

Fig 3 Program area select

64000 microprocessor development system in 6809 mnemonics. Full software listing is in Appendix a.

Fig 5 shows the function of the software.

3.1 Setting up the SSDA's

The SSDA's, as mentioned previously are the serial interfaces between the external data stream and the microprocessor. Because the SSDA's have many functions they need to be set up prior to operation. The SSDA "looks" like two memory locations to the microprocessor and depending on whether the microprocessor is reading or writing to the locations they will have different functions.

The following table shows the functions.

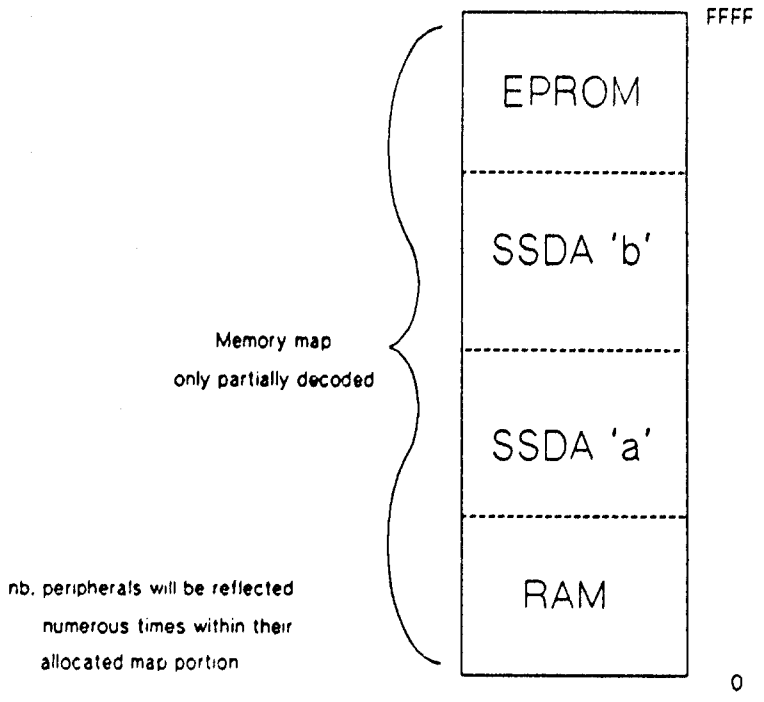

Fig 4 Memory map

table 1

address	ac1	ac2	r/w	function
0	X	X	0	Set up SSDA functions
0	X	X	1	Status of SSDA
1	0	0	0	Set up control reg. 2
1	0	1	0	Set up control reg. 3
1	1	0	0	Sync code data
1	1	1	0	TX data FIFO

3.2 Servicing the polled interupt

The processor continually polls the status register of both SSDA's to see whether the reciever registers are full. The first SSDA with a full receiver register is then serviced with the appropriate service routine. The service routines (for both

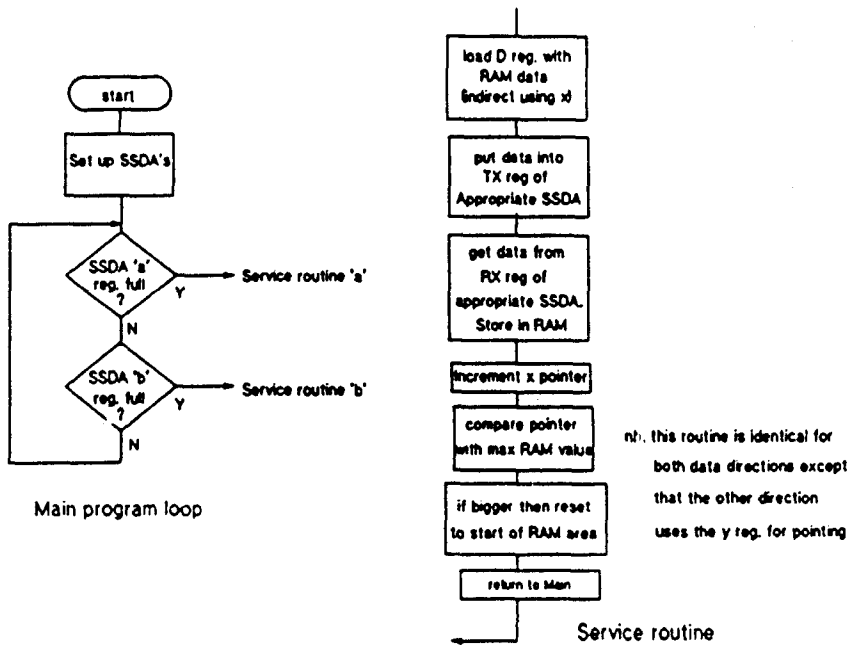

Fig 5 Functional software flowchart

directions) each have a pointer which points to an allocated area of RAM.

When the routine is invoked, the word (two bytes) which is currently pointed to is placed in the transmitter register in the appropriate SSDA. The two bytes which are in the receiver register then overwrite these two bytes in RAM. The pointer is then incremented.

After each increment of the pointer, the pointer value is checked against a value which is unique for the particular data rate. When the pointer is equal to this unique value then the pointer is reset to the start of the allocated buffer area thus creating a cyclic effect, the larger the value of the unique value then the larger the cycled buffer and thus the larger the delay. Fig 6, overleaf, shows this in more detail.

4.Conclusions/further work

The satellite delay box works as expected but one further area of expansion could be to utilise the thumbwheel switch to give a greater range of data rates than the four presently catered for. This could be achieved by tri-state buffering the lines of the thumbwheel switch onto the data bus and then reading this hexidecimal value and using this to select a buffer size variable from a look up table. This modification should be a fairly minor one.

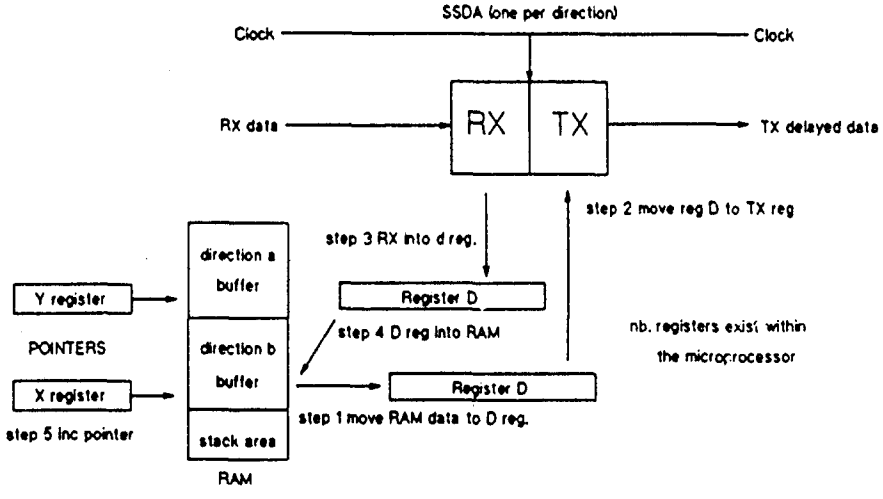

Fig 6 RAM cycle of service routine

5. Acknowledgements

I would like to thank Mr C.G.Slingsby and Mr H.A.Jeffreys for their help with this project.

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Abstract

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